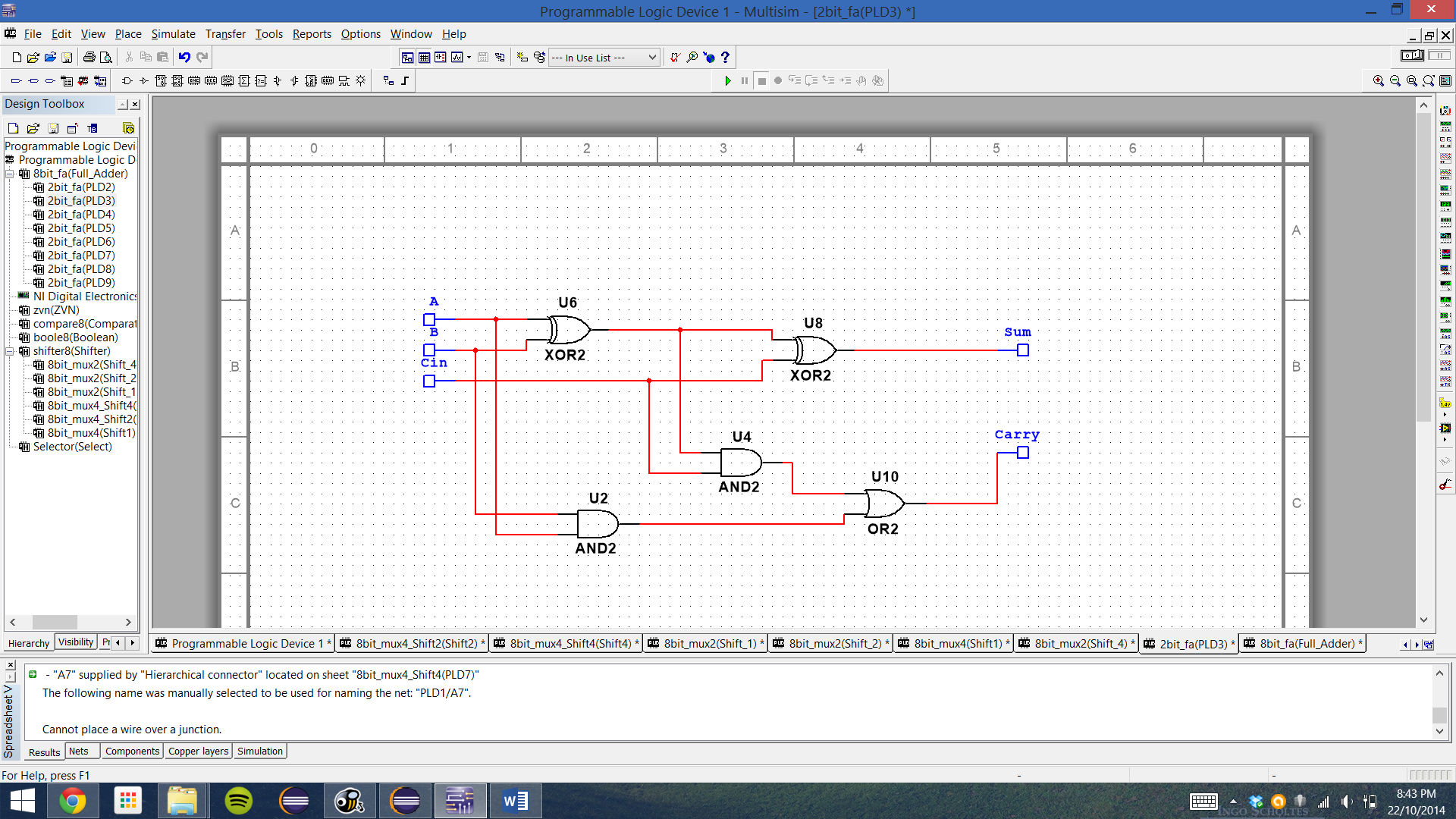
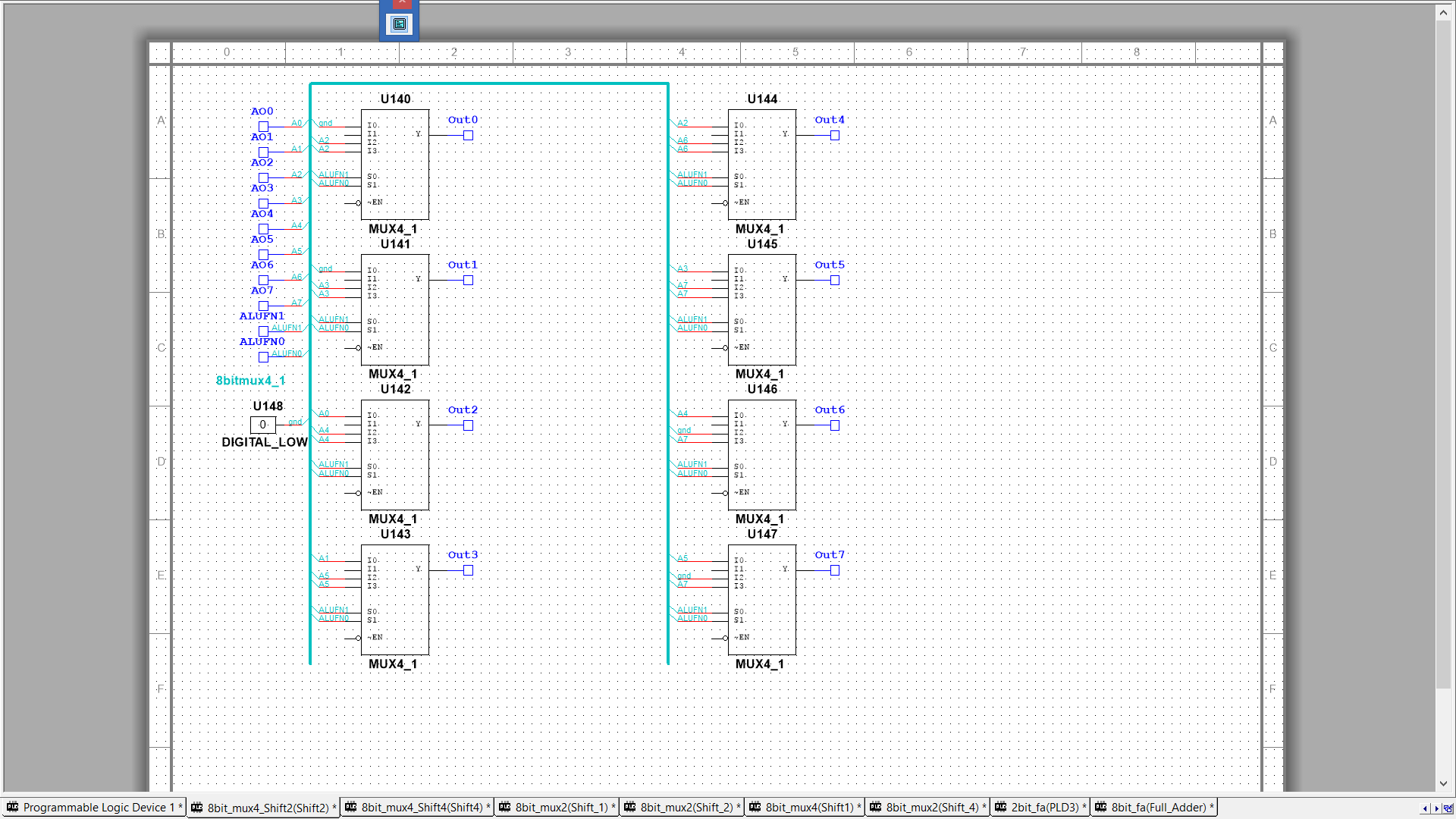
# Appendix

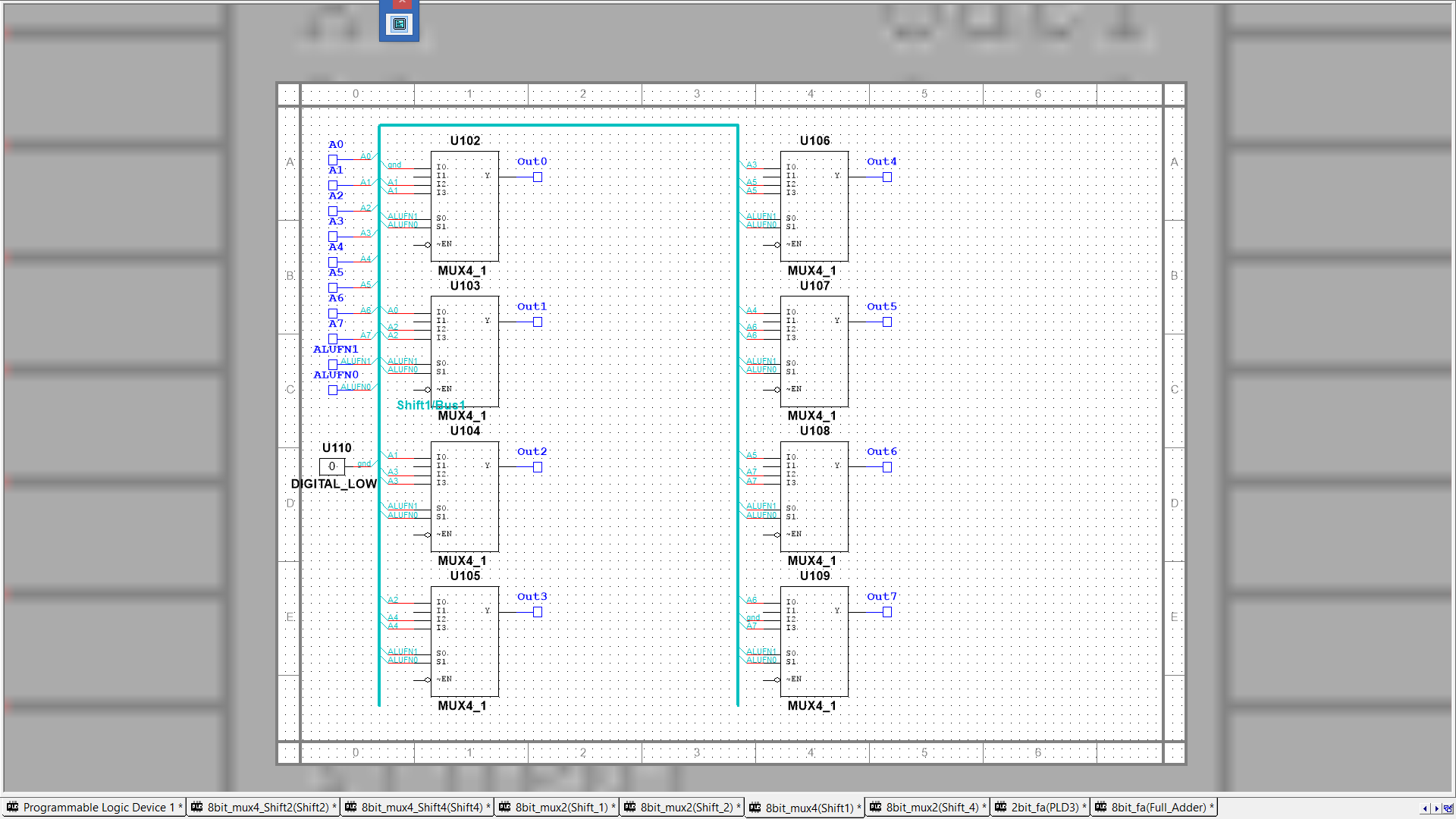
## Hierarchal Blocks



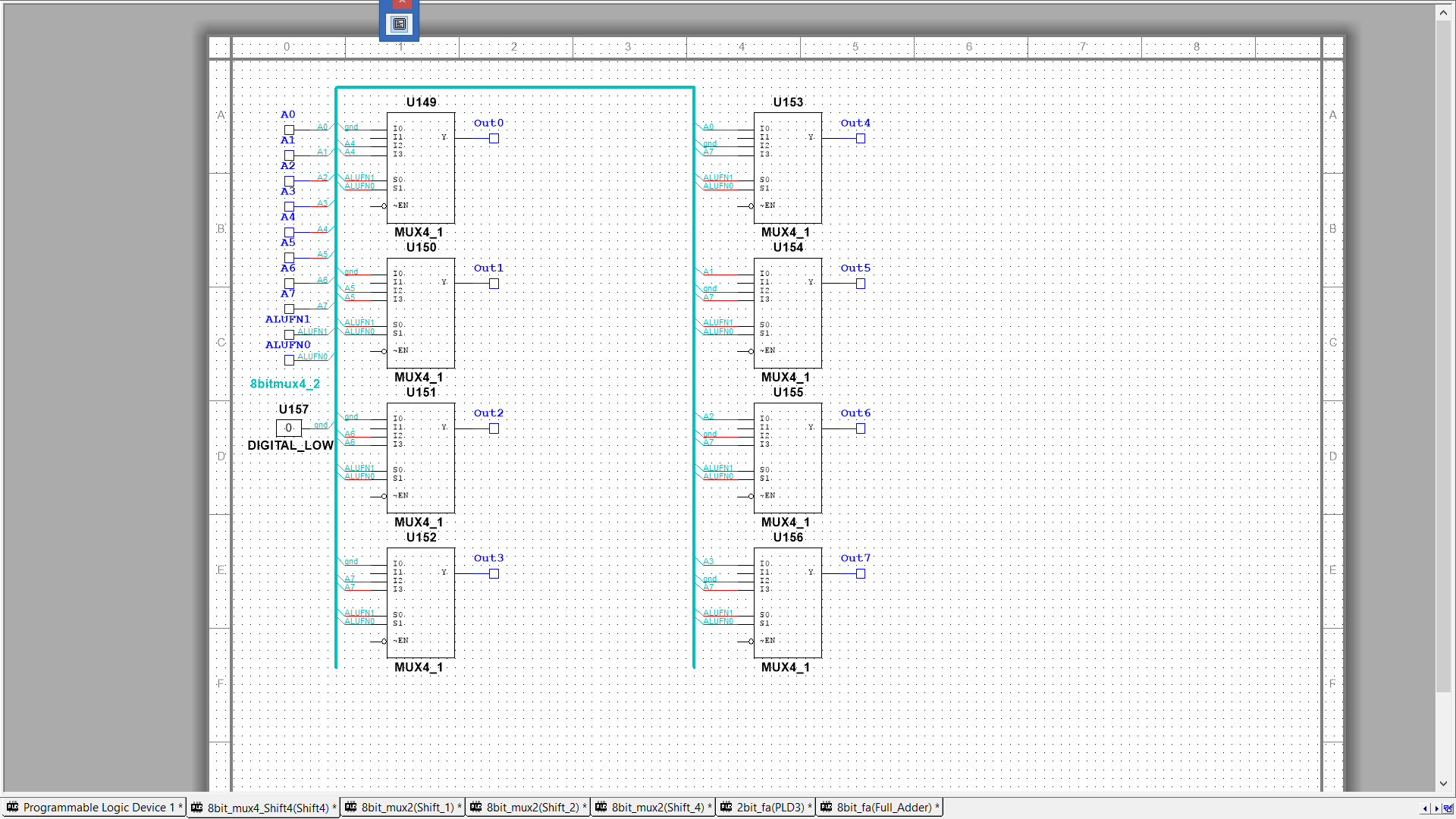
Block 1: Full Adder Block (2bit\_fa



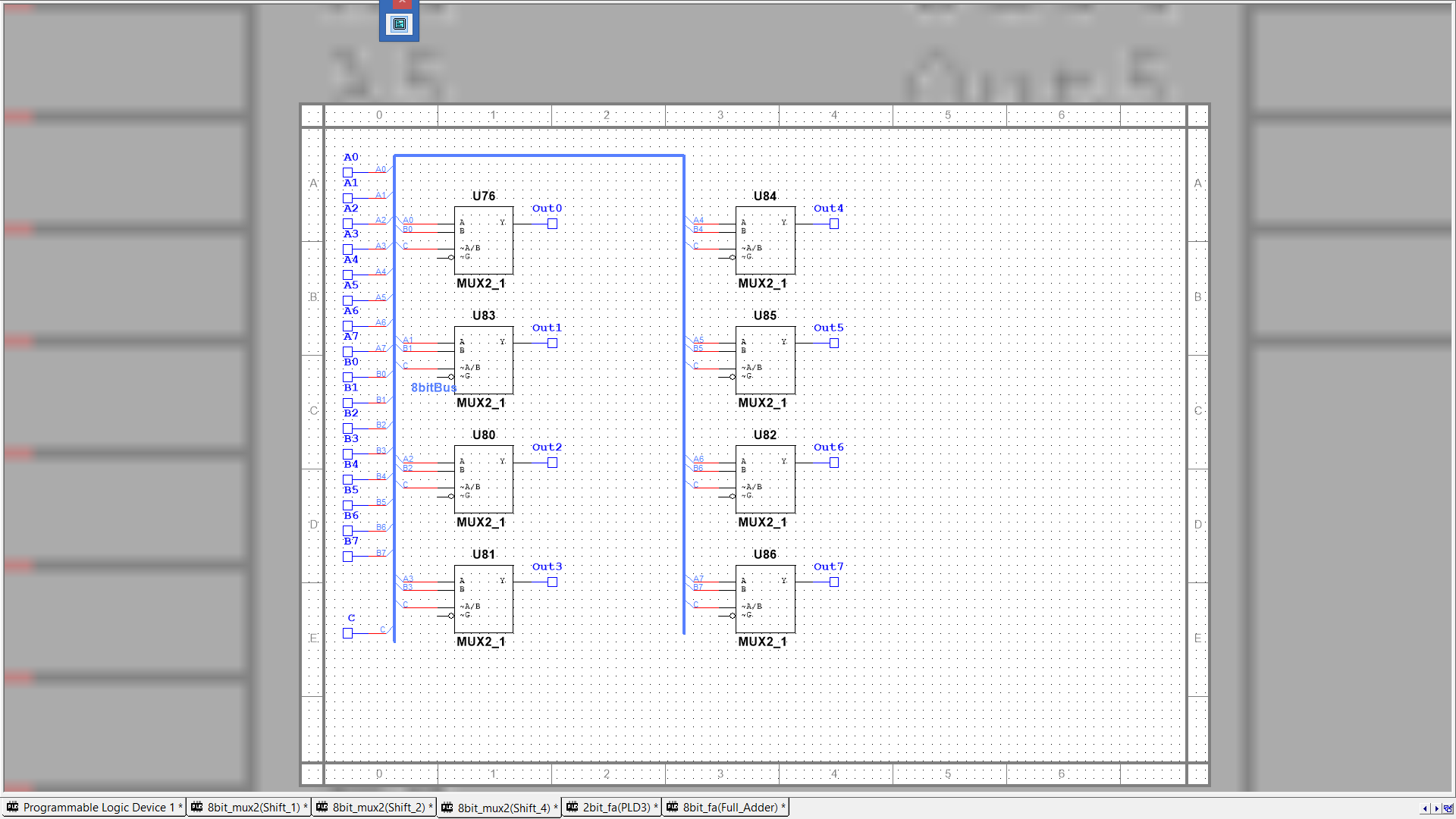
Block 2: 4 Mux 2 bit Shifter (8bit\_mux4\_Shift4)



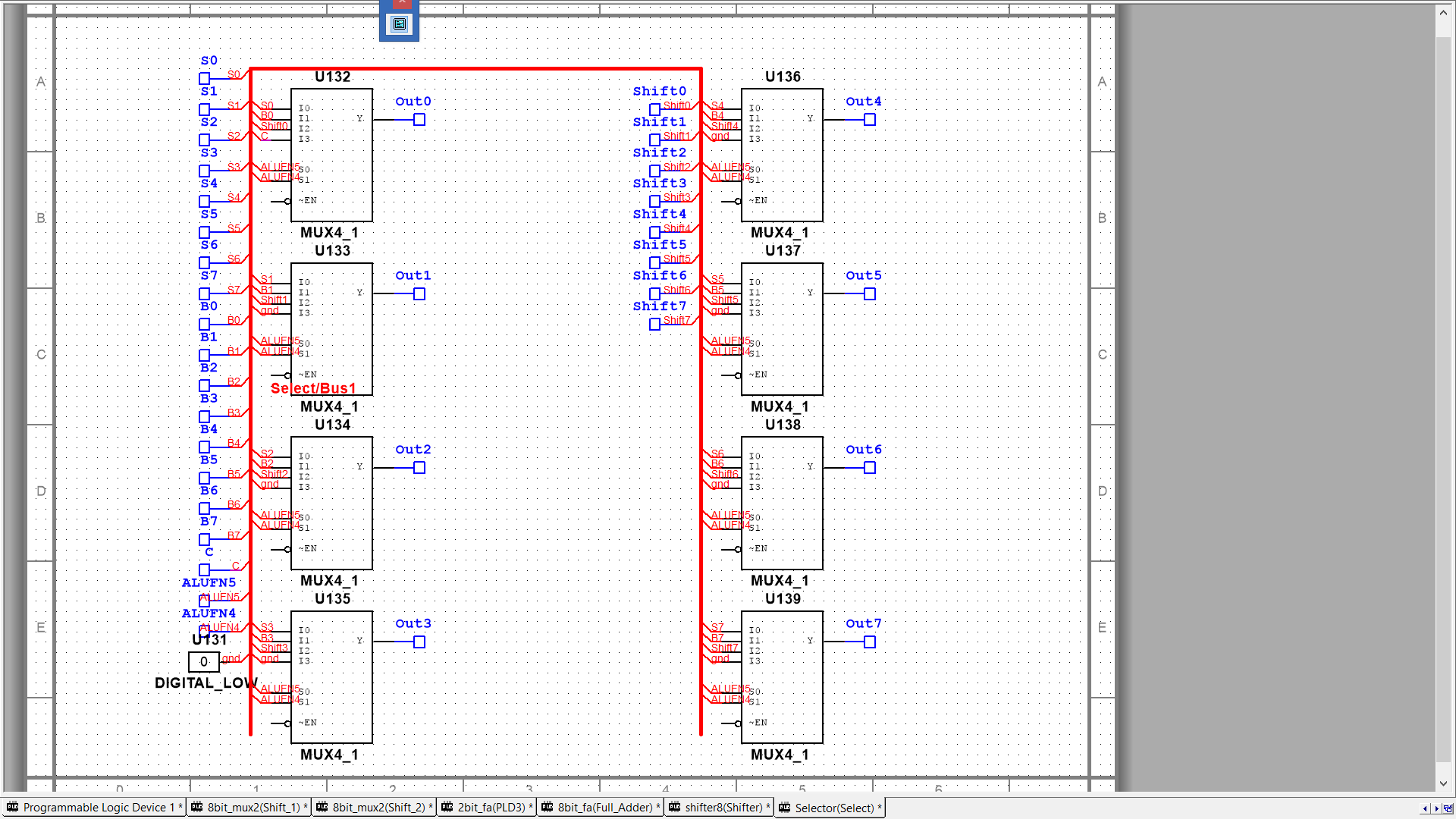
Block 3: 4 Mux 1 bit Shifter(8bit\_mux4(Shift1))



Block : 4 Mux 4 bit Shifter (8bit\_mux4\_Shift4)



Block : 2 Mux Shifter Selector (8bit\_mux2)



Block : PLD Selector(Select)